

Study of Catastrophic Latchup in the DSP2100 Signal Processor Chip for MLS

H. N. Becker
A. H. Johnston
T. F. Miyahira
Office 514

December 28, 2001

I. INTRODUCTION

This report summarizes the results of a series of tests to characterize catastrophic radiation-induced latchup in the DSP2100, which is used in three different applications on MLS. Latchup has been observed by JPL as well as by two other test organizations (Aerospace Corporation [Ref. 1] and ESA [Ref. 2]) in heavy-ion tests of DSP2100 devices. Recent tests were done on devices from the same date code used in MLS. Those results were reported in an internal JPL Test Report in April, 2001 [Ref. 3]. Heavy-ion data from those reports were used to calculate expected latchup rates for MLS. The estimated rates were 0.102 per year from heavy ions, and 1.7 per "design-case flare." Those rates apply to each part. Three DSP2100 devices are used on MLS, increasing the latchup probability by three.

Some of the latchup events observed in earlier tests caused catastrophic failure. The purpose of the tests described in this report is to determine whether current-detection-and-shutdown techniques can be used to reduce the likelihood of catastrophic failure after latchup occurs, thereby reducing the overall risk of failure from latchup on the MLS program. The older sets of data were taken using special power supplies that limit the maximum amount of current that can flow through a device during latchup, and also shut down the power after time periods of 10-100 ms. The special power control circuits were used to reduce the probability of catastrophic failure, eliminating the need to shut down the particle accelerator, break into the vacuum system, and change the device. This reduces test costs during latchup characterization tests, but provides little information about catastrophic failure because (a) the maximum current is limited to far lower values by the laboratory power supply system, and (b) the power is shut down within a narrow time interval.

Very little work has been done to investigate catastrophic latchup from space radiation. In most cases, devices that are sensitive to any form of latchup -- destructive or nondestructive -- are eliminated from serious consideration for use in space systems unless the threshold LET is high enough so that the latchup probability is very low. JPL requires

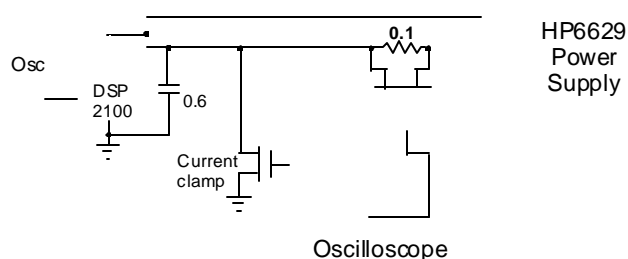
latchup probabilities of 10^{-4} per year or less in order to use latchup-prone devices without a waiver. One recent paper has shown that metallization failure appears to be the dominant failure mode for modern devices with small metallization dimensions [Ref. 4], but in most cases the specific failure mechanisms for catastrophic latchup have not been identified. Thus, the current work has to address several unknown aspects of latchup as it pertains to the use of parts that are highly sensitive to latchup in the space environment and for which no information is available about the nature of catastrophic damage.

II. TEST APPROACH

Tests of catastrophic latchup were done using a californium fission fragment source at JPL. Although the preferred way to do latchup evaluations is with more penetrating ions at high-energy accelerators, the cost of using such facilities is typically about \$600 per hour. The californium source allows a more elaborate series of tests to be done at far lower cost, and is the only practical way to do this type of study, which requires very lengthy test times. The californium fission fragments have less energy (with reduced penetration, a range of approximately 10 μm) compared to ions at accelerators, and thus are only approximately equivalent to the results with heavy ions. To partially compensate for this, the part was heated to about 50 °C during testing. This reduces the effective LET threshold for latchup by about 30% [Ref. 5], increasing the probability of latchup with the low-range californium ions and allowing the californium fission fragments to trigger latchup in more of the internal latchup-sensitive regions compared to tests at room temperature.

A special power control source was used for these tests that allowed measurement of each individual current waveform during the entire time period of the latchup event, and also provided for shutdown after a predetermined time interval. A simplified diagram of the power control system is shown in Figure 1. Power was supplied from a Hewlett-Packard 6629 power supply, which can provide currents up to two amperes. The force and sense lines of the power supply were used to establish

the correct voltage at the device, which was located in the vacuum chamber used for californium irradiations (only one side of the power supply connection is shown in the diagram for simplicity, but



an additional force/sense line pair was present in the negative lead connection to ground). Current was measured through a 0.1 ohm sampling resistor, using a special Tektronix differential amplifier with high common-mode rejection and low noise.

Figure 1. Diagram of power control circuit used for latchup testing.

Each waveform was stored in a digital oscilloscope, and transferred to a computer for later analysis. A pulse generator (not shown in the diagram) was used to set the time interval that latchup was allowed to persist before shutdown, as well as providing a short-duration input to the gate of the current clamp after that interval, which quenched the latchup condition. Tests were done under three different conditions, summarized in Table 1. The column labeled “Soak Time” refers to the time that the latchup condition was allowed to continue before the current clamp was triggered. The current limit during the test is the programmed maximum current limit value of the Hewlett-Packard power supply for Conditions A and B. For Condition C the current is the trigger level that was used to set a longer “soak time” for lower current events (Conditions B and C were used in combination, as discussed below). The 2-A current limit does not take into account the higher peak current from the 0.6 μ F capacitor that flows just after the onset of latchup. That capacitor matched the application circuit in MLS.

Table 1
Conditions Used for Latchup Tests

Condition	Latchup “Soak Time”	Current Limit During Test
A	2 sec	2 A

B	1 ms	2 A
C	0.5 sec	0.4 A

Tests were made under these conditions for several different devices. During the radiation tests the test device was operated with a clock input, but without any explicit programming or external diagnostics (*an extensive effort would have been required to develop the hardware and software required to implement more thorough tests, which was incompatible with the funds and schedule requirements*). Thus, it was not possible to determine whether the device continued to function properly after latchup occurred *during* the radiation tests. Functionality was determined by removing each device from the vacuum system after a number of latchup events -- from ~10 to 100 -- had occurred, and placing into the breadboard system that was developed by MLS during the design.

A wide range of equilibrium currents occurred during latchup, from approximately 30 mA to the 2 A limit of the Hewlett-Packard power supply. This is consistent with results for other complex devices, where there are literally thousands of internal latchup sites, with a wide range of equilibrium currents during latchup [Ref. 6]. In nearly all cases the current exhibited a fixed step just after latchup was initiated, continuing at that same level until the clamp circuit was triggered. In a few instances one or more additional stepped increases in current were observed during the “soak period”, suggesting that additional latchup paths had been triggered. This could occur either because of localized heating, or from additional latchup events triggered by californium particles. However, the mean time between events was approximately 6 minutes, and thus it is unlikely that two latchup events could occur during the very short time period that the devices were allowed to remain in a latched condition.

Alpha particles are also emitted by californium at a rate that is about 60 times higher than the rate for fission. The small incremental charge from the alpha particles could cause additional latchup sites to turn on after the extreme localized heating from the first latchup event raised the chip temperature, and this is the likely reason for the stepped increases in current

during the soak time. Small, randomly occurring current transients were evident on the current waveforms during latchup that may be due to current from the alpha particles, lending additional support to the assumption that alpha particles are responsible for exciting additional latchup sites in locally heated regions.

III. TEST RESULTS

A. Initial Results with 2-sec Soak Time and 2-A Current Limit

The first set of tests was done with a 2-second soak time (condition A in Table 1). Five different devices were tested. Table 2 summarizes the results. Three of the devices had been used in earlier radiation tests, either heavy ions at Brookhaven National Laboratory or high-energy protons at Indiana University, which will introduce some internal lifetime damage. There appeared to be some difference between the results for parts that were previously irradiated compared to results with fresh devices. That is consistent with the assumption that bulk damage in the substrate of the device reduces the amount of charge that is collected when the ion passes through the substrate. The lower charge may prevent some latchup sites from being triggered by the californium ions, making it difficult to compare results between fresh and previously irradiated parts.

As shown in the table, four of the five devices were no longer functional in the MLS test system after the latchup tests. The first device (#4400) was tested overnight, with a total of 472 latchup events. However, no intermediate functional measurements were done. Consequently we do not know how many latchup events had occurred prior to failure. Note further that because latchup involves bipolar elements within the CMOS device that the device will still exhibit latchup even after it is damaged to the point where it no longer functions properly. There are large numbers of internal latchup sites, and even if the conducting path to one site is damaged, other sites can be readily triggered into latchup. Thus, *electrically* damaged devices are not expected to exhibit any apparent difference in latchup sensitivity.

The second device failed after only 10 latchup events. The seventh latchup was a high-current

event, saturating the supply limit which (for that test only) was set to 1.22 A, not 2A. Thus, it is likely that the catastrophic failure occurred after 7 latchup events.

The third device was tested in two sequences. It was removed from the test after 13 latchup events, and still worked properly. It was then tested overnight (206 additional latchup events) and was no longer functional when it was removed from the test chamber the following morning. That particular device had been tested with protons before the latchup tests with californium were done, receiving a total dose of about 20 krad.

The fourth device failed after 17 latchup events. That was very similar to the results for the second device, which was also a “fresh” part with no previous radiation history.

The fifth device, #4526, had also been irradiated with protons before californium tests were done. It still operated after 55 latchup events, but the mean time between latchup events was longer, suggesting that significant damage had occurred because of the previous irradiation with protons. Thus, the fact that #4426 did not fail after 55 latchup events is quite likely the result of the reduced latchup sensitivity.

A sixth device, not shown in the table, failed after approximately three events. That device was in the chamber, waiting for the vacuum system to pump down. The operator was interrupted by a telephone call from the MLS program, which took about 15 minutes. A latchup event occurred during that time interval, and the device was destroyed.

Table 2
Devices Tested with Condition A

S/N	Total Latchup Events	Status at Test End	Current Limit	Part History
4400	472	destroyed	2 A	Previous radiation test
4402	10	destroyed	1.22 A	Fresh
4524	219	destroyed	2 A	Previous radiation test
4728	17	destroyed	2 A	Fresh

4526	55	OK	2 A	Previous radiation test
------	----	----	-----	-------------------------

Test results under Condition A indicate that devices with no previous radiation history will fail catastrophically after approximately 10 latchup events have occurred. High-current latchup events occurred for both “fresh” devices in the sequence of 10-17 events that preceded functionally testing. The implication is that only about 10% of the latchup events produce the internal conditions that cause immediate failure. A rudimentary statistical analysis shows that catastrophic latchup could occur for as few as 4.7 or as many as 18.4 events, with 95% confidence.

Results for parts that were previously irradiated are clearly different, which is expected because of displacement damage that reduces the amount of charge collected from the fission fragments, making it more difficult to initiate latchup. The test results with Condition A suggested that only the high-current events caused failure. That was used as the basis for the mitigation scheme discussed in the next subsection.

B. Results with “Two-Tier” Soak Time - Conditions B and C in Table 1

Two fresh devices were tested using a combination of conditions that was selected to emulate the conditions for the latchup detection and shutdown circuitry that is planned for implementation in MLS. Note, however, that these test conditions were set up in our laboratory with commercial test equipment, and did not use the specific circuit and software that is under development by MLS at this time. The two conditions are as follows:

1. For latchup currents > 400 mA, shut down the power system after the current flows for 1 ms (this limits the time interval for high current latchup events).
2. For latchup current ≤ 400 mA, shut down the power system after the current flows for 0.5 seconds. That time period is much longer because it must be implemented with software, not hardware, in the anticipated latchup

mitigation approach, although it was implemented in hardware for the radiation tests.

Each device was subjected to radiation tests over a time period of about 11/2 hours, during which approximately 10 latchup events were observed. The devices were removed from the vacuum system and tested with MLS hardware after each run; this was done to get better information about the statistics of latchup failure in the event that a failure occurred. After 2-3 short-duration tests with no post-irradiation failure, each device was tested overnight, adding approximately 100 additional latchup events before functional tests were done.

Both devices remained functional after more than 120 latchup events occurred. For each device, 11 of the latchup events exceeded 1 A. In the case of S/N 4756, 5 of the 11 high-current events saturated the power supply (2A). This is important because it is very likely that only the high-current events create the internal conditions that cause catastrophic failure.

Table 3
Results of “Two-Tier” Test Method on the DSP2100

Serial No.	Total Latchup Events	Events ≥ 400 mA	Events ≥ 1.0 A	Post-Test Status
4525	125	52	11 (5 were 2-A)	Functional
4756	122	46	11 (all 1-A)	Functional

Although only two devices were available for tests with the current control conditions that are anticipated for MLS, both devices sustained numerous latchup events without any obvious failure. About 40% of the latchup currents exceeded 400 mA. These results suggest that current limiting will be reasonably effective in reducing the incidence of catastrophic failure after latchup occurs.

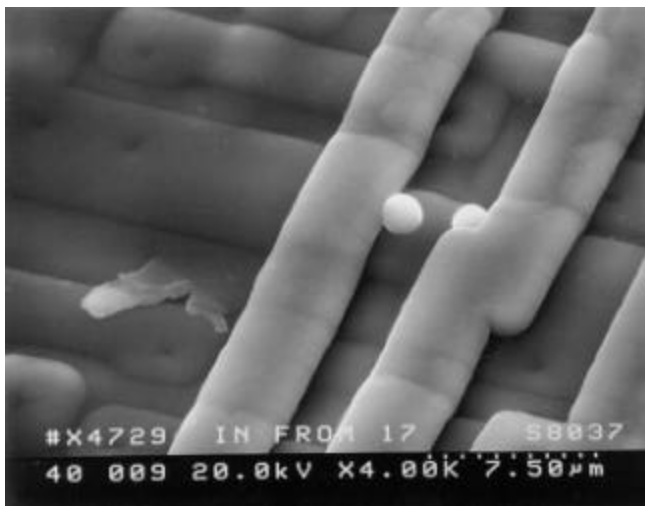
IV. DISCUSSION AND CONCLUSIONS

A. Damage from Latchup in the DSP2100

Mechanisms for failure from latchup have not been widely studied. As discussed earlier, a recent paper that will be published in the December 2001

issue of the Transactions on Nuclear Science showed that catastrophic failure in a modern analog-to-digital converter was due to ejected metallization after latchup [Ref. 5]. The metallization lines where failure occurred were $1 \times 0.5 \mu\text{m}$ in dimension, and currents between 150 and 200 mA were sufficient to cause such failures. Similar failure signatures were observed in the DSP2100. The photomicrograph in Figure 2 illustrates ejected metal in three different regions from a DSP2100 that had been subjected to numerous latchup events. The dimensions of the underlying metallization lines in the DSP2100 are $1.6 \times 0.6 \mu\text{m}$, a cross-sectional area that is about twice that of the metallization lines in the analog-to-digital converter that was studied in Reference 5.

At the left, an extended “tongue” of ejected metal from the first level of metallization can be seen; because of the amount of metal it is very likely that this event caused catastrophic failure. There are also two regions where small spheres of metal have been ejected. Because the dimensions of the metal



spheres are much smaller than that of the metal line, is quite likely that those regions did not produce failure in the device. The process will, however, produce voids in the metallization that may affect the device reliability in normal operation.

Figure 2. Scanning electron micrograph of a failed DSP2100

Similar effects were reported for the analog-to-digital converter that was studied in Reference 5. In that work a pulsed laser was used to initiate latchup that allowed direct determination of the region where latchup was initiated as well as real-time evaluation of

device operation. Some of the ejected metal spheres in that study did not produce open metal lines, even though there were large voids in the metallization.

B. Time Interval for Metallization Failure

The oscilloscope waveforms provide some information about the time period in which metallization damage is likely to occur. Many of the events that likely caused failure produced currents that immediately reach the 2-A maximum limit of the power supply. In those cases the oscilloscope waveforms do not provide much useful information about the latency time period between latchup initiation and failure. However, there are cases where a decrease in current occurs in the waveform during the “soak” period. Figure 3 shows an example. In this case the current showed a stepped decrease about 300 ms after the latchup occurred. The peak current for this waveform was about 650 mA. The decrease in current could be caused either by a catastrophic break in the metal, or by increase in the metal resistance due to metal ejection.

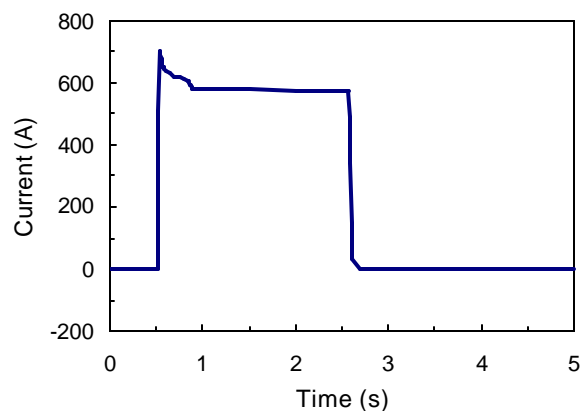


Figure 3. Discontinuity in current during latchup attributed to metallization line failure.

The waveform also shows higher current at time intervals below 200 ms. Most of the current waveforms, including some with currents above 1 A, showed nearly constant current conditions throughout the entire latchup time interval. The implication for the latchup event in Figure 3 is that the current would have to be shut down within about 100 ms in order to avoid damage. However, the fact that the two devices tested with the “two tier” current approach each sustained 11 latchup events above 400 mA without catastrophic failure suggests that the event in

Figure 3 is somewhat unlikely to occur. Nevertheless, it illustrates the difficulty of coming up with a successful scheme for avoiding catastrophic failure from latchup.

C. Power Control Conditions in MLS Applications

The application of the DSP2100 in MLS does not include any provision for current monitoring or power shutdown at the present time. However, MLS system designers are in the process of adding two modifications:

1. Addition of a current monitor and shutdown circuit that will sense a total power supply current condition > 0.4 A and shut down power to the power supply connection with a series connection within 1 ms (this corresponds to Condition C in Table 1), and
2. Modification of the software so that power to the device will be shut down if the DSP2100 becomes nonfunctional. The designers expect that this can be done with a maximum latency time of 0.35 sec, which is slightly less than the time period used for the tests done under Condition C in Table 1.

Note that condition (2) above does not directly sense latchup, but assumes that latchup will cause the DSP to lose normal functionality. That may not be true in all cases, and is one of the unknown risks for the “two-tier” approach for latchup mitigation. The reason for condition (2) is that the normal operating current in the DSP application varies over a wide range, making it impossible to use current sensing techniques for more moderate currents.

V. CONCLUSIONS AND PERSPECTIVE

A. Latchup Failure Probability with Implementation of Mitigation Circuitry and Software

Latchup in modern integrated circuits is a very complex issue [Ref. 6]. Even though a great deal of effort was spent in characterizing latchup in the DSP2100, the statistics of high-current latchup events and limited diagnostics are insufficient to make a definite statement about the probability of failure from latchup. Adding to the difficulty is the fact that mechanisms and conditions for catastrophic latchup have not been studied in detail.

Nevertheless, the tests described in this report strongly suggest that the mitigation approach proposed for MLS will significantly reduce the probability that a latchup event will cause immediate destruction of the device. The two devices that were subjected to the “two-tier” test, which emulates the mitigation approach that is under development for MLS, did not result in any failures even though about 250 latchup events occurred. The catastrophic latchup probability is at least a factor of 10 below the total latchup probability, provided that this mitigation approach is implemented.

Tests done with a two-second time interval suggest that even without current shutdown the probability that a latchup event actually causes failure is about 0.2 (with 95% confidence). Thus, the latchup mitigation approach does not have to be entirely successful as long as the software will eventually shut down the power as the device overheats. Note however that one DSP2100 device failed in less than 15 minutes in a laboratory test where the shutdown circuitry was inadvertently not working due to interruption of the operator.

B. Perspective on Latchup and Latchup Mitigation

The use of parts that are prone to any form of latchup for space applications is a highly questionable practice that is inconsistent with JPL policy. The latchup probability of the DSP2100 is three orders of magnitude higher than allowed by JPL policy. With the mitigation circuitry, it is possible to reduce the risk rating from high to medium, but not to “low” because of the inherent difficulty of implementing and testing the latchup mitigation technique and the risk of catastrophic failure if the approach is only partially successful. Note also that latent metallization damage is likely to occur for some latchup events that are not catastrophic.

In this instance latchup mitigation was a last resort because the MLS Program uses a unique digital-signal processor for which no suitable alternative is available without extremely costly changes in design and software. The additional latchup testing that was done for this device support the assertion that the latchup failure probability is at least a factor of ten lower with the proposed

mitigation approach. However, latchup mitigation is difficult to implement. Additional radiation tests of the DSP2100 are highly recommended using the hardware and software techniques after they are implemented in order to verify that they are effective in eliminating catastrophic latchup failure.

VI. REFERENCES

1. R. Koga, *et al.*, "The Risk of Using SEE Sensitive COTS Digital Signal Processors in Space," IEEE Trans. Nucl. Sci., 43, 2982 (1996).
2. R. Harboe-Sorenson, *et al.*, "The Single Event Upset Response of the Analog Devices ADSP2100A Digital Signal Processor," RADEC91 Proceedings, IEEE Document 91TH0400-2, p. 457.
3. F. Irom, *et al.*, "Single Event Effects Tests for the First Five Part Types Used on the MLS Program," internal JPL report, May, 2001.
4. T. F. Miyahira, *et al.*, "Catastrophic Latchup in Advanced Analog-to-Digital Converters," presented at the 2001 Nuclear and Space Radiation Effects Conference, Vancouver, Canada, July 16-20, 2001; accepted for publication in the IEEE Trans. on Nucl. Sci., December, 2001 (*in press*).
5. A. H. Johnston, B. W. Hughlock and R. E. Plaag, "The Effect of Elevated Temperature on Single-Particle Latchup," IEEE Trans. Nucl. Sci., 38, 1435 (1991).
6. A. H. Johnston, "The Influence of VLSI Technology Evolution on Radiation-Induced Latchup in Space Systems," IEEE Trans. Nucl. Sci., 43, 505 (1996).